IEEE Electron Devices Society
International Mini-Colloquium

May 7-8, 2009

Institute of Physics
Maria Curie-Skłodowska University
Lublin, Poland

Programme
Thursday, May 7, 2009

11:15 Welcome Note

11:30 Sorin Cristoloveanu
Physics and Technology of Multiple-Gate MOSFETs
Institute of Microelectronics, Electromagnetism and Photonics (IMEP, UMR 5130)
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The nano-size multiple-gate SOI MOS transistor is the ideal candidate for the microelectronics future, including the transition from micro- to nano-electronics. The MOSFET scaling is intrinsically easier in SOI than in bulk Si, where it is becoming a desperate issue. The key condition is to utilize ultra-thin bodies and to open the SOI family to any kind of semiconductor, strained or not, on any type of dielectric. The aim of this presentation is to illustrate the improvement of the electrostatic control achieved by the association of several gates. Two, three or four gates can collaborate for enabling enhanced performance, functionality, flexibility and scaling. Several device architectures (planar or vertical double gates, Ω or Π topologies, 4-gate and gate-all-around transistors) and related technologies will be discussed by comparing their merits and feasibility. Since the device operation is governed by 3-D effects, we will describe the typical coupling mechanisms along the longitudinal, lateral and vertical directions. Various applications of multiple-gate transistors will be evoked.

12:30 Mikael Östling
Present status of SiC power electronic devices
KTH-Royal Institute of Technology, SE-164 40 Kista, Sweden

Silicon carbide electronic devices are already commercially available in a few application areas such as high voltage rectifiers and emerging rf power amplifiers. Over the past 15 years a very rapid progress of both materials and device quality has been seen and is very encouraging for application market. Prototype devices show amazing improvement each year in all device categories as well as a markedly improved wafer quality. However, materials defect issues are still limiting economically viable production of large area devices with high yield. In this paper a thorough review of progress in SiC device process technology presents the state-of-the art SiC devices as well as new application areas.

Friday, May 8, 2009

9:30 Enrico Sangiorgi
Simulation of self-heating effects in SOI MOS architectures

ARCES-DEIS University of Bologna and IUNET, Via Venezia 260, 47023 Cesena, Italy

Self-heating effect is expected to become an increasing problem for the forthcoming technological nodes of silicon-based semiconductor technology, due to the use of new architectures as the silicon-on-insulator (SOI), replacing the traditional bulk CMOS device. Thin silicon layers over thermally insulated SiO_2 buried-oxide, feature a thermal conductivity much lower than that of silicon bulk. Severe self-heating effect detrimentally impacts the carrier mobility and therefore the saturation drain current.
In this talk we discuss self-heating effects in different SOI architectures: n-channel planar single- and double-gate as well as FinFET transistors, designed in order to have the same electrical isothermal characteristics: threshold voltage, transconductance and a good tolerance to the short-channel-effects.

10:30 Henryk M. Przewłocki
A new class of photoelectric methods to determine MOS system parameters: The zero photocurrent methods

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New model of photoelectric phenomena taking place in the MOS system near the zero photocurrent point has been developed and will be characterized shortly. A series of new photoelectric measurement methods of MOS structure parameters, based on this model, will be presented. In particular, measurement methods will be discussed of the effective contact potential difference (ECPD) in the MOS system, as well as of the effective charge at the dielectric-semiconductor interface. This photoelectric ECPD measurement method is the most sensitive and accurate of the existing methods of this parameter determination. It will be shown that distributions over the gate area of the local values of MOS system parameters can also be determined by photoelectric methods. This way interesting features and interesting differences between various MOS systems will be demonstrated. Comparisons will be shown between results obtained using the above mentioned methods and other photoelectric and electrical measurements.

11.30 Closing of the Mini-Colloquium

The IEEE EDS International Mini-Colloquium will be held in the **Aula Fizyki** hall of the **Institute of Physics, Maria Curie-Skłodowska University, Lublin, ul. Radziszewskiego10.**